## REMARKS

This is a full and timely response to the outstanding final Office Action mailed December 4, 2003. Claims 1 – 4, 6 – 8, 10 - 11 and 19 - 33 remain pending. Reconsideration and allowance of the application and presently pending claims are respectfully requested.

**Rejections under 35 U.S.C. §103**

The Office Action indicates that claims 1 – 4, 6 – 8, 10 – 11 and 19 - 33 stand rejected under 35 U.S.C. 103(a) as being unpatentable over *Iida* in view of *Yamazaki*. Applicant respectfully traverses the rejection.

The Office Action indicates that *Iida* discloses:

> A first conductor (8 (of T2), fig. 25) formed through said first wafer;
> A first conductor insulating layer (9b (of T2), fig. 25) formed through said first wafer, said first conductor insulating layer engaging said first conductor and disposed between said first conductor and material of said first wafer, said first conductor insulating layer being formed of dielectric material; and
> A first insulating layer (9a (inner wall of T1), fig 25) formed at least partially through said first wafer and spaced from said first conductor insulating layer, said first outer insulating later being formed of dielectric material.
> A second outer insulating layer (9a (outer wall of T1), fig. 25) formed through said first wafer (14, Fig. 25) and spaced from said first outer insulating layer;
> Wherein said first conductor extends through said first wafer form said first side to said second side (col. 10, Ins. 11 – 24).

Applicant respectfully asserts that even if *Iida* disclosed the limitations recited above in the Office Action, Applicant's claims recite different features/limitations; therefore, the Office Action does not present a prima facie case of obviousness. For this reason alone, Applicant respectfully asserts that the rejection is improper and that the claims are in condition for allowance.

Respectfully referring the Examiner's attention to claim 1, that claim recites:

> 1. A system for electrically isolating a portion of a wafer comprising:
> a first wafer having a first side and an opposing second side;
> ***a first conductor extending through said first wafer from said first side to said second side***;
> a first conductor insulating layer extending through said first wafer, said first conductor insulating layer engaging said first conductor and disposed between said first conductor and material of said first wafer, said first conductor insulating layer being formed of dielectric material; and
> ***a first outer insulating layer extending through said first wafer from said first side to said second side and spaced from said first conductor insulating layer such that said first outer insulating layer at least partially electrically isolates said first conductor from portions of the first wafer located outside said first outer insulating layer***, said first outer insulating layer being formed of dielectric material. (Emphasis added).

Applicant respectfully asserts that *Iida* and *Yamazaki*, either individually or in combination, are legally deficient for the purpose of rendering obvious claim 1, because neither of the references teaches nor reasonably suggests at least the features/limitations emphasized above in claim 1. Specifically, the references do not teach or reasonably suggest at least "a first conductor extending through said first wafer from said first side to said second side," in combination with "a first outer insulating layer extending through said first wafer from said first side to said second side and spaced from said first conductor insulating layer such that said outer insulating layer at least partially electrically isolates said first conductor from portions of the wafer located outside said first outer insulating layer."

With respect to *Iida*, the Office Action indicates that element 8 of FIG. 25 corresponds to Applicant's first conductor. Applicant respectfully disagrees with this contention. Turning to column 10, lines 11 – 24 of *Iida*, element 8 of FIG. 25 is described as a polysilicon trench filled region 8. Thus, element 8 is not a "first conductor." Additionally, as shown in FIG. 25, element 8 is not "extending through said first wafer from said first side to said second side" as recited in claim 1.

The Office Action directs the Applicant's attention to column 10, lines 11 – 24 of *Iida* for the proposition that *Iida* teaches said first conductor extending through said wafer from said first side to said second side.

However, that portion of *Iida* discloses:

> The seventh embodiment is illustrated in a cross-sectional view in FIG. 25 and in a plane view in FIG. 25, wherein FIG. 25 is a cross-sectional view taken along line D—D' in FIG. 26. As illustrated in these figures, the $P^+$ base region 5 is completely surrounded by the trench T2, i.e., the silicon oxide film 9*b*, and the polysilicon trench filled region 8 within the trench T2 is set to be high in impurity concentration and grounded. In this arrangement, the polysilicon trench filled region 8 within the trench T1 can be set to be low in impurity concentration, the collector parasitic capacity of the transistor can be reduced, and as a result, the frequency characteristics (operation speed) can be improved while the withstand voltage can be lowered and the size can be reduced.

Applicant has thoroughly reviewed the *Iida* reference, including that portion set forth above, and has not been able to identify any portion of *Iida* (including the drawings) that disclose "a first conductor extending through said first wafer from said first side to said second side" as alleged in the Office Action. Since it appears that the *Iida* reference has been misconstrued with respect to at least this particular feature, Applicant respectfully asserts that the rejection is improper and should be removed.

The Office Action also indicates that Applicant's first outer insulating layer is disclosed by element 9A of FIG. 25 of *Iida*. Applicant respectfully notes that it appears that the Office Action has relied on Applicant's previous claim language, which recited that the first outer insulating layer was "formed at least partially through said first wafer." In response to the first non-final Office Action, however, Applicant amended claim 1 to recite, in pertinent part, "a first outer insulating layer extending through said first wafer from said first side to said second side . . .". Since element 9A of *Iida* does not teach or reasonably suggest such a first outer insulating layer, Applicant respectfully asserts that the rejection is improper for at least this additional reason.

Applicant respectfully notes that *Yamazaki* also does not teach or reasonably suggest at least the features/limitations that have been indicated above as lacking in *Iida*. Thus, the combination of *Iida* and *Yamazaki* is legally deficient for the purpose of rendering obvious the presently rejected claims. Therefore, Applicant respectfully asserts that claim 1 and its dependent claims are in condition for allowance.

Turning now to claim 20, which was added in the previous Response, that claims recites:

> 20. A system comprising:
> a first semiconductor wafer having a substrate material; and
> ***a via structure adapted to provide electrical communication through the first wafer, the via structure comprising:***
> first and second conductors having insulating layers to form a barrier with the substrate; and
> ***an outer insulating layer formed about both the first and second conductors to electrically isolate the first and second conductors from the substrate material.***
> (Emphasis Added).

Applicant respectfully asserts that *Iida* and *Yamazaki*, either individually or in combination, are legally deficient for the purpose of rendering obvious claim 20, because at least the features/limitations emphasized above are not taught or reasonably suggested by the references. Specifically, Applicant respectfully asserts that neither *Iida* nor *Yamazaki* teaches or reasonably suggests at least "a via structure adapted to provide electrical communication through the first wafer" in combination with "an outer insulating layer formed about both the first and second conductors to electrically isolate the first and second conductors from the substrate material." Therefore, Applicant respectfully asserts that claim 20 is in condition for allowance.

Because claims 21 – 29 depend from and incorporate all the features/limitations of claim 20, Applicant respectfully asserts that these claims also are in condition for allowance.

Additionally, these claims recite additional features/limitations that also may serve as an independent basis for patentability. By way of example, claim 21 recites:

> 21. The system of claim 20 further comprising a second semiconductor wafer stacked to the first wafer, wherein the via structure provides electrical communication between the first wafer and the second wafer.

Applicant respectfully asserts that the cited art of record does not teach or reasonably suggest the features/limitations of independent claim 20 in combination with "a second semiconductor wafer stacked to the first wafer, wherein the first via structure provides electrical communication between the first wafer and the second wafer." For at least this additional reason, Applicant respectfully asserts that claim 21 is in condition for allowance.

Applicant notes that the limitations of claim 20 and its dependent claims do not appear to be specifically addressed in the pending Office Action.

Turning now to claim 30, that claim recites:

> 30. A system, comprising:
> ***a plurality of semiconductor wafers forming a wafer stack***, each wafer comprising:
> a substrate material; and
> a via structure in the substrate material, ***the via structure providing electrical communication from one wafer to another wafer, each via structure comprising a first conductor having an insulating layer***, a second conductor having an insulating layer and being electrically insulated from the first conductor, ***and an outer insulating layer formed around both the first and second conductors to electrically isolate the first and second conductors from the substrate material***.
> (Emphasis Added).

Applicant respectfully asserts that the cited art of record does not teach or reasonably suggest the features/limitations emphasized above in claim 30. Specifically, the cited art, either individually or in combination, does not teach or reasonably suggest "a plurality of semiconductor wafers forming a wafer stack," "the via structure providing electrical communication from one wafer to another wafer," and "an outer insulating layer formed around both the first and second conductors to electrically isolate the first and second

conductors from the substrate material." For at least this reason, Applicant respectfully asserts that claim 30 is in condition for allowance.

Since claims 31 – 33 depend from and incorporate all the features/limitations of claim 3, Applicant respectfully asserts that these claims also are in condition for allowance. Additionally, these claims recite the features/limitations that also may serve as an independent basis for patentability.

For example, claim 31 recites:

> 31. The system of claim 30 wherein electrical signals propagate from the via structure of one wafer to the via structure of another wafer.

As another example, claim 32 recites:

> 32. The system of claim 30 wherein electrical signals propagate through one of the via structures from an outer surface of one wafer to a location defined between two wafers.

As a further example, claim 33 recites:

> 33. The system of claim 30 wherein electrical signals propagate through the wafer stack through the via structure.

Applicant respectfully asserts that the cited art of record does not teach or reasonably suggest at least the features/limitations recited in claims 31 – 33, respectively. Therefore Applicant respectfully asserts that these claims are in condition for allowance.

Applicant notes that the limitations of claim 30 and its dependent claims do not appear to be specifically addressed in the pending Office Action.

**Prior Art Made of Record**

The prior art made of record has been considered, but is not believed to affect the patentability of the presently pending claims.

## CONCLUSION

In light of the foregoing amendments and for at least the reasons set forth above, Applicant respectfully submits that all objections and/or rejections have been traversed, rendered moot, and/or accommodated, and that the now pending claims 1 – 4, 6 – 8 and 10 – 11, and 19 - 33 are in condition for allowance. Favorable reconsideration and allowance of the present application and all pending claims are hereby courteously requested. If, in the opinion of the Examiner, a telephonic conference would expedite the examination of this matter, the Examiner is invited to call the undersigned attorney at (770) 933-9500.

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail, postage prepaid, in an envelope addressed to: Assistant Commissioner for Patents, P. O. Box 1450, Alexandria, VA 22313-1450, on 1/20/04.

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Signature